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DC to AC Multi level Inverter using Bi-directional Switch

Mr. G. Sasi Kumar

Associate Professor, VNRVJIET

Abstract: This paper report on new multilevel inverter uses five controlled switches, eight diodes and two capacitors to get five level ac output. The new inverter uses five controlled switches as other Multi level inverters use eight controlled switches. Multilevel inverters offer high power capability associated with lower output harmonics and lower commutation losses. Their main drawback is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. This work presents a new multilevel inverter topology using an H-bridge output stage with a bidirectional auxiliary switch. The proposed topology attains an multi-level output with 37.5% reduction of main switches required as compare with conventional multi-level inverters. The circuit is simulated using MATLAB Simulink software.

Key Words: H-Bridge Inverter, Auxiliary switch, Total Harmonic Distortion.

I. INTRODUCTION

The various types of multilevel inverter topologies presented in the literature [1] show a number of characteristics in common, giving them some clear advantages over bi-level converters, like reduction in the commutation frequency applied to the power components, reduction in the voltages applied to the main power switches, enabling operation at higher load voltages and transient voltages automatically limited.

The main drawback associated with the multilevel invertersis their circuit complexity, requiring a high number of power switches. They also require a more number of auxiliary dc levels, provided either by independent supplies or, more commonly, by a cumbersome array of capacitive voltage dividers. In this case, ensuring that the dc voltages are kept in equilibrium is another factor that increases the complexity of the modulator circuit. Multilevel converters were used only in some high power applications such as high power motor drivers in marine, mining, or chemical industries applications, high power transmission, power line conditioners, etc. [2]. The continuing development of high power high switch frequency devices such as insulated-gate bipolar transistors (IGBTs) working at 3.3, 4.5, and 6.5 kV, and insulated-gate commutated thyristors (IGCT) working at 4.5 or 6 kV, has improved overall converter performance, renewing the interest in multilevel topologies, that may be able to compete in the market with the standard two-level pulsewidth modulation (PWM) converters at lower power ranges [3]. Initially, the main interest was concentrated in three-level configurations [13][14] but recently fourand five-level converters have also been reported. The new converter topology used in the power stage offers an important improvement in terms of lower component count and reduced layout complexity when compared with the five-level converters presented in the literature [7],[8].

This work proposes a new converter topology, presented in Fig. 1. This topology includes an H-bridge with an auxiliary bidirectional switch, diodes, capacitor and power supply. Thistopology is used in the design of the five-levelDC-AC inverter output presented below.

II. POWER STAGE

A. Circuit Configuration

Fig. 1 shows the complete power circuit used in the five-level inverter. The H-bridge is formed by the four main power devices, S1 to S4 and four diodes D1 to D4. A capacitor voltage divider, formed by C1 and C2 provides a half supply voltage point, node A in Fig. 1. The auxiliary switch, formed by the controlled switch S5 and the four diodes, D5 to D8, connects the center point of the left hand half-bridge to node A.

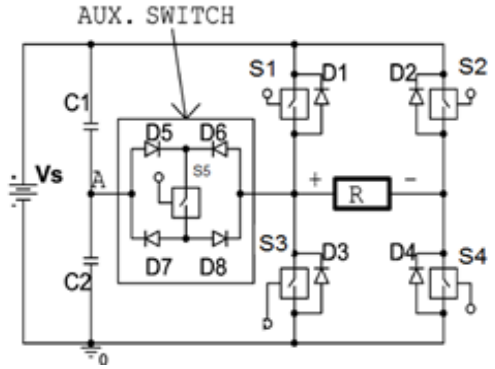

Fig1: H-Bridge inverter with Bidirectional switch

B. Stage Advantages

Table I shows the number of components required to implement a five-level inverter using the new topology and other three multi-level inverters: the diode clamped and the capacitor clamped configurations can be

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considered as the standard multilevel stages, and a new and highly improved multilevel stage, the asymmetric cascade configuration Output waveform acrossa resistive load is same for all topologies. Table1.provides No. of components used in each topology for producing five level Ac output wave form.

1) Main power switches:
The new topology achieves a 37.5% reduction in the number of main power switches required, using only five controlled power switches instead of the eight required in any of the other three configurations. The auxiliary switch voltage and current ratings are lower than the ones required by the main controlled switches.

Table I Comparison between Four Different Five Level Inverter Topologies

Multilevel inverter type	H-Bridge auxiliary switch	Diode clamped	Capacitor clamped	Asymmetric cascade
Main controlled switches	4	8	8	8
Auxiliary controlled switch	1	0	0	0
Diodes	8	20	8	8
capacitors	2	4	10	2

2) Auxiliary devices (diodes and capacitors):
The new configuration reduces the number of diodes by60% (eight instead of 20) and the number of capacitors by 50% (two instead of four) when compared with the diode clamped configuration. The new configuration reduces the number of capacitors by 80% (two instead of 10) when compared with the capacitor clamped configuration.

The new configuration uses no more diodes or capacitors that the second best topology in the Table1, the asymmetric cascade configuration. Additionally, since the two capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multilevel configurations.

C. Power Stage Operation

The required five voltage output levels (Vs, Vs/2, 0, -Vs/2, -Vs) are generated as follows:

1) Maximum positive output, Vs: S1 is ON, connecting the load positive terminal to Vs, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vs. Fig.2 shows the current paths that are active at this stage.

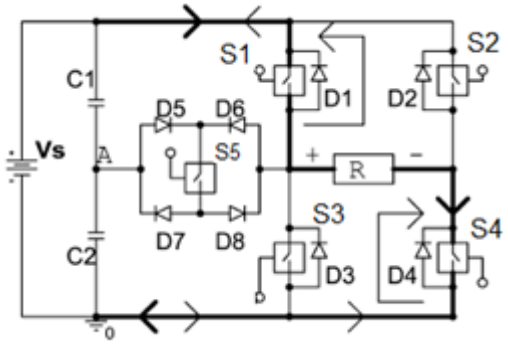

Fig2: Switching combination required to generate output voltage level Vs

2) Half-level positive output, Vs/2: The auxiliary switch, S5 is ON, connecting the load positive terminal to point A, through diodes D5 and D8, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vs/2. Fig.3 shows the current paths that are active at this stage.

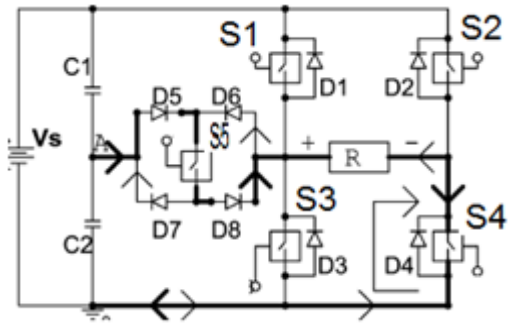

Fig3: Switching combination required to generate output voltage level Vs/2

3) Zero output: The two main switches S3 and S4 are ON, short-circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Fig.4 shows the current paths that are active at this stage.

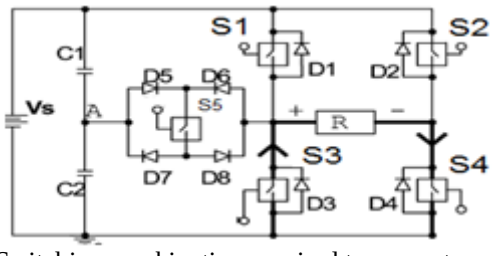

Fig4: Switching combination required to generate output voltage level zero

4) Half-level negative output, -Vs/2: The auxiliary switch, S5 is ON, connecting the load positive terminal to point A, through diodes D6 and D7, and S2 is ON, connecting the load negative terminal to Vs. All other controlled switches are OFF; the voltage applied to the load terminals is –Vs/2. Fig. 5 shows the current paths that are active at this stage.

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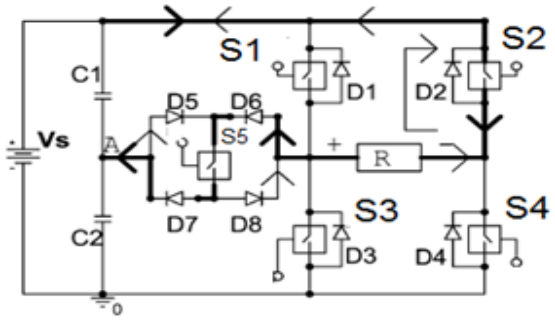

Fig5: Switching combination required to generate output voltage level –Vs/2

5) Maximum negative output: S2 is ON, connecting the load negative terminal to Vs, and S3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is (-Vs). Fig.6 shows the current paths that are active at this stage.

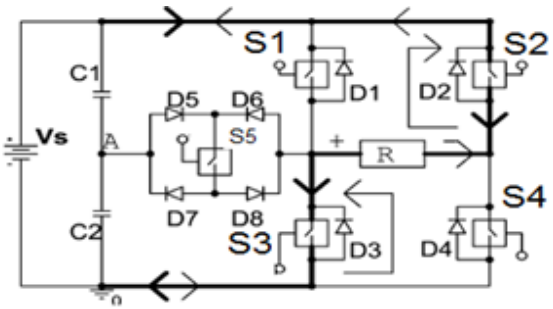

Fig6: Switching combination required to generate output voltage level –Vs

Table II lists the switching combinations that generate the required five output levels (Vs, Vs/2, 0, -Vs/2, -Vs).In this configuration the two capacitors in the capacitive voltage divider are connected directly across the dc bus, and since all switching combinations are activated in an output cycle, the dynamic voltage balance between the two capacitors is automatically restored.

Table II Switching Combinations Required to Generate the Five Level Output Waveform. At Any Instant Two Devices Are On Different Time Periods

S1	S2	S3	S4	S5	V_{RL}
on	off	off	on	off	V_S
off	off	off	on	on	$V_S/2$
off	off	on	on	off	0
off	on	off	off	on	$-V_S/2$
off	on	on	off	off	$-V_S$

IV SIMULATED RESULTS

The model of the new multilevel single phase inverter is simulated by using Matlab Simulink tool show in Fig8. Switching pulses for all the devices shown in Fig.7.The system tested with resistive load observe the input voltage, output voltage, output current in Fig9, Fig10 and Total harmonic distortion

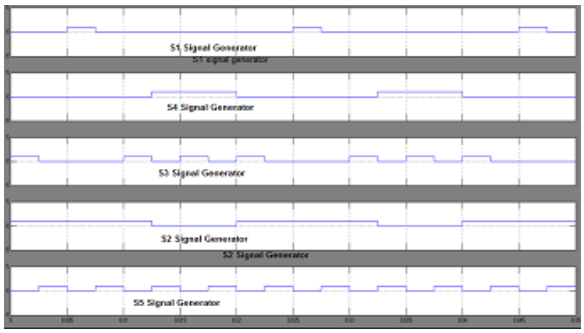

Fig7.Switching pulses for five devices

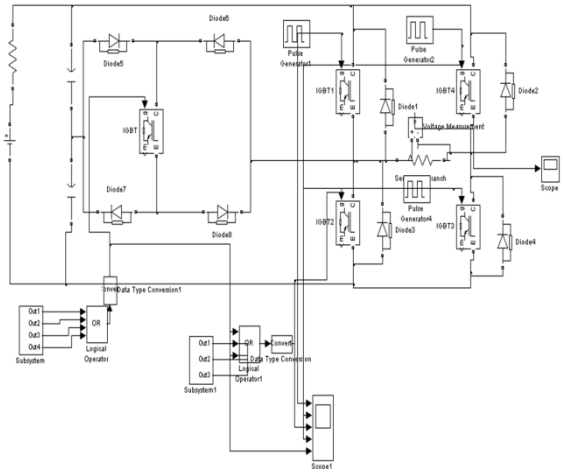

Fig8. New multi-level inverter Simulink diagram

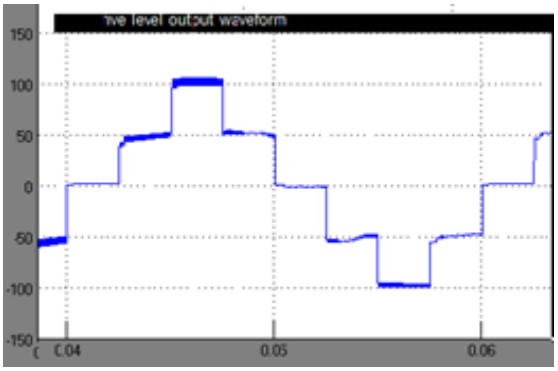

Fig.9. Simulated output voltage wave form across Resistive load

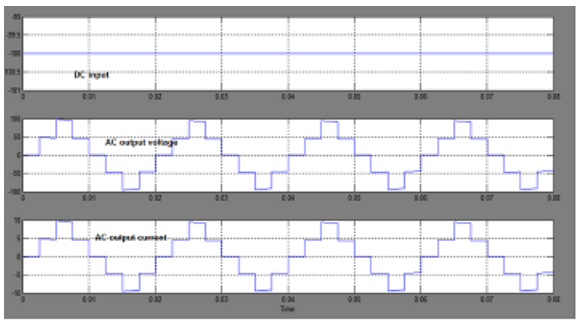

Fig.10. Simulated input voltage, output voltage and output current wave form across Resistive load

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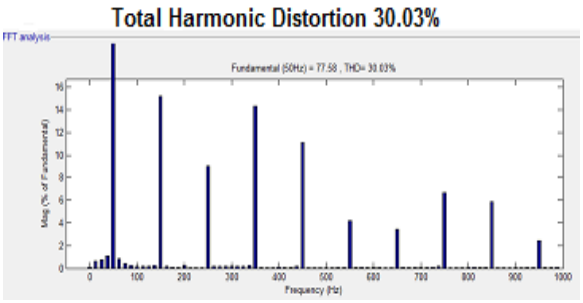

V. CONCLUSION

The new multilevel topology with the bidirectional auxiliary switch produced the required five-level output using only five power switches, and only one centre tap provided by two capacitors. To reduce Total Harmonic Reduction using filter circuit and PWM techniques. Next aim to develop the Proto type model for multi level inverter using FPGA controller.

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